Remarks

The above-referenced application has been reviewed in light of the Examiner's Final Office Action dated August 2, 2007, which makes final the rejections set forth in the Office Action dated January 24, 2007 (hereinafter, "the Office Action"). Claims 1, 3 and 12 have been amended. Therefore, Claims 1-20 are currently pending in this application. The Examiner's reconsideration of the rejections is respectfully requested, particularly in view of the above amendments and the following remarks.

In accordance with the Office Action, Claims 1-8 stand rejected under the judicially created doctrine of non-statutory double patenting. Claims 1 and 3 have been amended. In addition, it is respectfully requested that any rejections under this doctrine be held in abeyance until there is an allowable claim. In the present case, all of the currently pending claims are further rejected under 35 U.S.C. § 103(a). Accordingly, a Terminal Disclaimer, or the alternative cancellation of all claims rejected under the doctrine, may be timely filed upon the Examiner's indication of allowable subject matter.

In accordance with the Office Action, Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,918,040 to Jarvis in view of Applicant's Admitted Prior Art ("AAPA"). Claims 1, 3 and 12 have been amended. Support for these amendments is inherent in the Specification as originally filed. No new matter has been added. In addition, AAPA has been clarified with respect to translational artifacts.

Amended Claim 1 recites, *inter alia,* "A digital system comprising: a master circuit, which includes a circuit to detect clock delay . . . and a slave circuit . . . sends to the master circuit an input clock signal as a feedback signal of the output clock signal . . . wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to a variable initialization parameter corresponding to the detected delay."

The '040 to Jarvis is generally directed towards a method of coordinating the timers of two processors. The method of Jarvis detects and coordinates the timers of two networked processors by increasing the lesser of two timer values to match the greater value. Each of Jarvis' two processor circuits requires its own circuit to detect timer values, even though just the one that sees a lesser timer value takes action. That is, each of Jarvis' circuits is a "master" and neither is a "slave".

The '040 falls short with respect to various elements of each of Applicant's presently pending claims. Jarvis lacks "a slave circuit" as recited in Claim 1. Further, the method of Jarvis fails to teach or suggest "detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to a variable initialization parameter corresponding to the detected delay", as recited in Claim 1.

The Examiner relies on AAPA to show "slave circuit . . . sends to the master circuit an input clock signal as a feedback signal of the output clock signal", and other elements of Claim 1. AAPA has been amended to correct several translational artifacts. The corrected AAPA does not support "a feedback signal", which would necessarily be part of a feedback loop. As set forth in AAPA, the prior art required manual predetermination of a fixed delay and permanently stored the fixed delay in ROM, for example. *See, e.g.,* AAPA at page 4, lines 18-21.

At page 11 of the Office Action, last paragraph, the Examiner makes a rejection of Claim 1 while deferring to the later rejection of Claim 12 for the requisite motivation to combine. Beginning at page 14, last paragraph, the Examiner makes the rejection of Claim 12 while resting the motivation to combine on Applicant's Background section. Continuing at page 15 of the Office Action, 2nd paragraph, the Examiner relies on Applicant's Background section by stating, "These initial parameters are computed once synchronization is achieved". This is a misinterpretation of Applicant's Background section. To the contrary, Applicant's Background section shows that prior art methods first retrieved the fixed initial parameters from ROM in order to achieve synchronization, rather than *vise-versa*.

That is, Applicant's amended Claim 1 recites, *inter alia,* "wherein the circuit to detect clock delay . . . detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to a

variable initialization parameter corresponding to the detected delay". AAPA neither teaches nor fairly suggests that these "initial parameters are computed once synchronization is achieved" as suggested by the Examiner, much less setting a "variable initialization parameter corresponding to the detected delay" between an output clock signal and an input clock signal as effectively claimed by Applicant. Similarly, each of amended Claims 3 and 12 recite features comparable to those of amended Claim 1.

Accordingly, Claims 1, 3 and 12 are neither taught nor suggested by U.S. Patent No. 5,918,040 to Jarvis in view of AAPA, whether taken alone or in combination with any of the other references of record in this case.

Conclusion:

Accordingly, it is respectfully submitted that amended independent Claims 1, 3 and 12 are in condition for allowance for at least the reasons stated above. Since the remaining dependent claims each depend from one of the above claims and necessarily include each of the elements and limitations thereof, it is respectfully submitted that these claims are also in condition for allowance for at least the reasons stated, as well as for reciting additional patentable subject matter. Thus, each of Claims 1-20 is in condition for allowance. All issues raised by the Examiner having been addressed, reconsideration of the rejections and an early and favorable allowance of this case are earnestly solicited.

Respectfully submitted,

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